REMARKS

Status of the Application

Claims 1-15 were pending as of the present Office Action, which states that:

Claim 9 is rejected under the first paragraph of 35 U.S.C. § 112;

Claims 4 and 5 are objected to for various informalities; and

Claims 1-8 and 10-15 are rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,191,408 to Shinotsuka et al. (hereinafter "Shinotsuka") in view of U.S. Patent No. 6,133,862 to Dhuse et al. (hereinafter "Dhuse").

By this Amendment, new claims 16-20 have been added.

In addition, the present Office Action sets forth various objections of the abstract, drawings, and specification of the present application.

Drawings

Fig. 15

The indication, in the Office Action, that Fig. 15 should be designated by a legend such as "Prior Art" is noted. Accordingly, a Letter to the Official Draftsperson is being filed concurrently herewith submitting a corrected version of Fig. 15 that includes a designation of "Prior Art". In addition, the Letter to the Official Draftsperson being filed concurrently herewith also includes a corrected version of Fig. 1 that includes an item number "1" for the "vertical scanning unit" as required on page 3 of the present Office Action as part of the objection to the specification.

Objection under 37 CFR 1.83(a)

The indication, in the Office Action, that the drawings are objected to under 37 C.F.R. 1.83(a) is respectfully traversed based on the following.

The basis for the present objection is an allegation that a "solid-state image-sensing device as claimed in claim 1, wherein the first and second pixels have an identical circuit configuration" is not shown in the drawings. This allegation is respectfully traversed. Attention is drawn to the second embodiment, particularly paragraphs 56 and 66 of the specification. Paragraph 66 specifically sets forth that the circuit shown in Fig. 7 is used as compensation pixels (which satisfy the definition of "a second pixel") and ordinary pixels (which satisfy the definition of "a first pixel"). Paragraph 56 specifically sets forth that the area sensor [i.e. solid-state image-sensing device (see para. 13)] of the second embodiment, including the circuit shown in Fig. 7, is configured as shown in Fig. 1.

Thus, Fig. 1 shows a solid-state image-sensing device wherein the first and second pixels can have identical circuit configurations according to at least one embodiment of the present invention. Therefore, it is respectfully requested that the objection to the drawings under 37 C.F.R. 1.83(a) be reconsidered and withdrawn.

Abstract and Specification Objections

Abstract

The objection to the abstract because the reference numerals are not in parentheses, citing MPEP § 608.01(b), is respectfully traversed. A review of MPEP § 608.01(b) revealed no such requirement. While it is acknowledged that MPEP § 1826 requires abstracts of PCT applications have reference numerals in parentheses in accordance with PCT Rule 8, since the present application is not a PCT application, there is no known basis for the present objection of the abstract. Accordingly, it is respectfully requested that the objection to the abstract be reconsidered and withdrawn.

Specification

The objection to the specification due to several minor errors contained therein is noted. Accordingly, the present amendment includes several changes to the specification to improve the grammar and form thereof. In addition, as mentioned above, the Letter to the Official Draftsperson being filed concurrently herewith also includes a corrected version of Fig. 1 that includes an item number "1" for the "vertical scanning unit" as required on page 3 of the present Office Action as part of the objection to the specification. Therefore, it is respectfully requested that the objection to the specification be reconsidered and withdrawn.

35 U.S.C. § 112 Rejection

The rejection of claim 9 under the first paragraph of 35 U.S.C. § 112 is respectfully traversed based on the following.

The basis for the present rejection is an allegation that "[t]he first and second pixels are only discussed and shown as having inherently differing circuit configurations, due to their differing functions." This allegation is respectfully traversed. Attention is drawn to the second embodiment, particularly paragraphs 56 and 66 of the specification. Paragraph 66 specifically sets forth that the circuit shown in Fig. 7 is used as compensation pixels (which satisfy the definition of "a second pixel") and ordinary pixels (which satisfy the definition of "a first pixel").

Thus, the specification clearly sets forth a single circuit configuration, in at least the second embodiment and in Fig. 7, that can be used as the first pixel and the second pixel.

Accordingly, it is respectfully requested that the rejection of claim 9 under the first paragraph of 35 U.S.C. § 112 be reconsidered and withdrawn.

35 U.S.C. § 103(a) Rejection

The rejection of claims 1-8 and 10-15 under 35 U.S.C. § 103(a) over Shinotsuka in view of Dhuse is respectfully traversed based on the following.

In setting forth the rejection of claims 1-8 and 10-15, the present Office Action relies on a combination of Shinotsuka and Dhuse. The proposed combination of Shinotsuka and Dhuse includes disclosure of respective image sensors 1 and 114. Both Shinotsuka and Dhuse subject the output of the respective image sensors 1 and 114 to some sort of post-processing in order to compensate for variations, such as those that can occur during manufacturing, among the physical properties of the pixels. In the case of Shinotsuka, one embodiment includes a correcting device 6 as a post processor that compensates for variations among inflection points of respective photosensors 4 of the image sensor 1. In the case of Dhuse, the output of the pixels of the pixel array (e.g. 502_A to 502_N) are output to correlated double sampling (CDS) units 514_A to 514_N for post processing in order to compensate for "fixed effects caused by manufacturing differences for each pixel."[1] Thus, the combination of Shinotsuka and Dhuse teaches post-processing, such as processing an output of an array or matrix of pixels, for compensating for variations among various properties of the pixels.

Dhuse also discloses reference pixels, however the reference pixels do not compensate for variations among various properties of the pixels. Instead, the reference pixels are used for compensating for variations (or "noise") from the power supply. The reference pixels 400, 516, 518 simply store and pass along voltages that are supplied by the power supply, allowing for calculation of power supply noise (see step 606, Fig. 6).

So, considering that the combination of Shinotsuka and Dhuse both use post-processing for compensating for variations among various physical properties of the pixels themselves, such as is done by the correcting device 6 of Shinotsuka pointed out in the

[1] Dhuse, col. 4, lines 59-60.

present rejection, and considering that the reference pixels also pointed out in the present rejection of Dhuse are used for a different purpose altogether, absent the benefit of improper hindsight there is no motivation for one skilled in the art to modify the Shinotsuka device in order to incorporate the extensive amount of circuitry involved with the correcting device 6 into a single reference pixel.

The present rejection of claims 1-8 and 10-15 relies on a combination of Shinotsuka and Dhuse, indicating that it would have been obvious "to provide the correction circuitry **6** of Shinotsuka in the form of a [reference] pixel, and to dispose this second pixel in the array of original pixels **4**"[2] since Dhuse shows reference pixels. However, as shown above, there is no motivation for making such a modification to the Shinotsuka device, i.e., there is no motivation for combining Shinotsuka and Dhuse as set forth as a basis for the present rejection. Since establishing a *prima facie* case of obviousness requires *inter alia* "some suggestion or motivation...to modify the reference or to combine the reference teachings,"[3] the proposed combination of Shinotsuka and Dhuse cannot render claims 1-8 and 10-15 *prima facie* obvious.

Accordingly, it is respectfully requested that the rejection of claims 1-8 and 10-15 under 35 U.S.C. § 103(a) over Shinotsuka in view of Dhuse be reconsidered and withdrawn.

New Claims

New claims 16-20 have been added to provide a more adequate basis for protection of the invention. No new matter has been added.

Claim 16 is an independent claim, and claims 17-20 depend from claim 16. Accordingly, the following discussion of claim 16 applies equally to claims 17-20.

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[2] Office Action, page 4, lines 22-23 (August 14, 2002).
[3] MPEP 2143 (8th ed.).

Claim 16 recites:

> A solid-state image-sensing device comprising:
> a first pixel, which includes a photoelectric conversion element, for generating a first pixel output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element;
> a second pixel for generating a second pixel output signal,
> wherein the second pixel output signal is used for reducing signal noise that is caused by the first pixel; and
> a reading circuit for reading out the output signals of the first and second pixels.

Both Shinosutka and Dhusa fail to disclose or suggest a pixel for generating a signal that is used for reducing signal noise that is caused by another pixel. Instead, as pointed out above, both Shinosutka, Dhusa, and the proposed combination thereof teach compensating for signal variations, such as noise, caused by a pixel using a post-processing means. Therefore, none of Shinosutka, Dhusa, and the proposed combination thereof can render obvious claim 16 or claims 17-20 which depend from claim 16.

CONCLUSION

In view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

This Amendment increases the number of independent claims by one from two to three, increases the total number of claims by five from fifteen to twenty, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be

construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document, other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The following is a marked-up version of the changes to the abstract, specification, and claims which are being made in the attached response to the Office Action dated August 14, 2002.

IN THE SPECIFICATION:

Paragraph **[0008]** beginning on page 2 and ending on page 3.

[0008] However, the circuit configuration described above has the following disadvantage. As shown in Fig. 15, the output signals from the individual pixels are amplified by the MOS transistors Q1 provided one for each column. If the characteristics of these MOS transistors Q1 vary among them, the output signals from the pixels belonging to different columns are amplified by different amplification factors. Accordingly, although there is no variation among the output signals from the pixels arranged in an identical column, there appear variations among the output signals from the pixels arranged in an identical row because those output signals are amplified by different amplification factors. As a result, when an image is reproduced from the output signals obtained from an area sensor like this, variations in the amplification ~~factor~~factors among the MOS transistors Q1 that are provided, one for each column, cause fixed pattern noise that looks like vertical stripes.

Paragraph **[0019]** on page 9.

[0019] Now, ~~how~~ the operation of the area sensor configured as described above ~~operates~~ will be described. Suppose that, now, image sensing is going to be performed to obtain an image that constitutes a

frame. First, the vertical scanning circuit 1 feeds, by way of the line 3-0, a signal ϕV to the gates of the MOS transistors T3 (described later) provided in the compensation pixels G10 to Gm0. At this time, the output switching circuit 9 connects together the output side of the differential amplifier circuit 12 and the input side of the line memory 10 and in addition the switch SW is turned off so that the output signals fed from the differential amplifier circuit 12 will be fed to the line memory 10.

Paragraph **[0072]** on page 26.

[0072] Another example of the configuration of the compensation pixels used in cases where the ordinary pixels are configured as shown in Fig. 7 will be described below. In the configuration shown in Fig. 8, such circuit components as serve the same purposes as in the pixel shown in Fig. 7 are identified with the same reference numerals, and their explanations will be omitted.

Paragraph **[0081]** on page 29.

[0081] In the pixel shown in Fig. 9, such circuit elements, signal lines, and the like as serve the same purposes as in the pixel shown in Fig. 3 are identified with the same reference numerals, and their explanations will be omitted. The pixel shown in Fig. 9 is obtained by additionally providing, in the pixel shown in Fig. 3, a MOS transistor T5 having its gate connected to the node between the drain and gate of the MOS transistor T1 and having its source connected to the gate of the MOS transistor T2, and a capacitor C having one end connected to the node between the gate of the MOS transistor T2 ~~ad~~and the source of the MOS transistor T5 and receiving the direct-current voltage VPS at the other end.

Paragraph **[0087]** on page 31.

[0087] An example of the configuration of the compensation pixels used in cases where the ordinary pixels are configured as shown in Fig. 9 will be described below with reference to Fig 10. In the configuration shown in Fig. 10, such circuit components as serve the same purposes as in the pixel shown in Fig. 9 are identified with the same reference numerals, and their explanations will be omitted.

Paragraph **[0092]** on page 32.

[0092] The compensation data thus output is used as signals representing variations in characteristics among the MOS transistors Q1 (Fig. 1) connected to the signal lines 5-1 to 5-m (Fig. 1). By configuring the compensation pixels in largely the same manner as the ordinary pixels ~~in this way~~, it is possible to obtain compensation data that reflects the potential state of the photoelectric conversion circuits; that is, it is possible to obtain compensation data under largely the same conditions under which the ordinary pixels operate.

Paragraph **[0100]** on page 35.

[0100] In this example, the compensation pixels are configured, just like the compensation pixel of the third example of the first embodiment, as shown in Fig. 6. Thus, the compensation pixel of this example is configured and operates just as described previously in connection with the first embodiment, and therefore no description thereof will be given anew. Configured in this way, the compensation pixel of this example has an even simpler configuration than that of the third example (Fig. 5) of this embodiment, thanks to the elimination of the photoelectric conversion circuit. This helps make the compensation pixels smaller in size than the ordinary pixels, and thereby ~~minimize~~minimizes the extent to

which the size of the compensation pixels limits the size of the ordinary pixels.

Paragraph **[0124]** beginning on page 43 and ending on page 44.

[0124] In this example, the compensation pixels are configured, just like the compensation pixel of the third example of the first embodiment, as shown in Fig. 6. Thus, the compensation pixel of this example is configured and operates just as described previously in connection with the first embodiment, and therefore no description thereof will be given anew. Configured in this way, the compensation pixel of this example has an even simpler configuration than that of the third example (Fig. 8) of this embodiment, thanks to the elimination of the photoelectric conversion circuit. This helps make the compensation pixels smaller in size than the ordinary pixels, and thereby ~~minimize~~minimizes the extent to which the size of the compensation pixels limits the size of the ordinary pixels.

IN THE CLAIMS:

New claims 16-20 have been added.